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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,090	10/29/2003	Seung-Jae Chung	5649-1152	6639

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,090	CHUNG ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) for the REPUBLIC OF KOREA Application 2002-87246, filed 12/30/2002. The certified copy has been filed in parent Application No. 10/696,090, filed on 10/29/2003.

Specification

The abstract of the disclosure is objected to because it fails to comply with the proper format for an abstract of the disclosure, by exceeding the required length. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 4 recite the limitation "the first sub logic circuit unit". There is insufficient antecedent basis for this limitation in the claim.

Claim 1 recites the limitations "wherein the core block generates core output data for the plurality of ports response to output data for the plurality of output ports input to a plurality of input ports of the core block", which render the claim indefinite

Claim 4 recites the limitations "wherein the core block generates core internal data responsive to output data from the input ports and wherein the core block is configured to output the core internal data during scan testing and to selectively generate core output data for the output ports responsive to the core internal data or to test vector serial input data from the vector input terminal", which render the claim indefinite.

The claims are generally narrative and indefinite, failing to conform to current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors. The Applicant is advised to rewrite the claims as required and avoid excessive language (i.e., output data for the plurality of output ports input to a plurality of input ports) in describing the claimed invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the

applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Whetsel (US Patent No. 6,877,122) ISSUED: April 5, 2005, FILED: December 21, 2001.

Regarding independent Claims 1, 13, 15, 20, Whetsel discloses a test architecture and method 601 for accessing wrappers (307-308) within an integrated circuit to test intellectual property (IP) cores via the wrappers, which reside at the boundary of a core and provides a way to test the core and interconnections between the cores, Figures 3, 6, 8, comprising:

A core block (cores 1-3) connecting three individual wrappers 307-309 configured for dynamic simulation testing, wherein the core block having an associated plurality of output ports (SO-1, SO-2, SO-3) and generating core output data (serial output, SO) corresponding to output ports (SO-1, SO-2, SO-3).

An input side sub logic circuit unit (input linking circuitry 602) receives a serial input (SI 604) for dynamic simulation testing coupled to the input ports (SI-1, SI-2, SI-3) of the core block (cores 1-3) that generates sub data for the input ports. The wrapper serial outputs (SO-1, SO-2, SO-3) are also input to the input linking circuitry 602.

MUX unit, such as multiplexers (608-610), that selectively provides connections between the serial inputs (SI-1, SI-2, SI-3) of wrappers 307-309 and signals SI 604,

(SO-1, SO-2, and SO-3). Multiplexers 608-610 receive linking control (SELSI-1, SELSI-2, SELSI-3) inputs from Link bus 606, Figure 6B.

Regarding independent Claims 4, 14, 16, 21, Whetsel discloses a test architecture and method 601 for accessing wrappers (307-308) within an integrated circuit to test intellectual property (IP) cores via the wrappers, which reside at the boundary of a core and provides a way to test the core and interconnections between the cores, Figures 3, 6, 8, comprising:

A core block (cores 1-3) connecting three individual wrappers 307-309 configured for dynamic simulation testing, wherein the core block having an associated plurality of output ports (SO-1, SO-2, SO-3) and generating core output data (serial output, SO) corresponding to output ports (SO-1, SO-2, SO-3). In addition, Whetsel discloses the core block is configured to output the core internal data corresponding to (SO-1, SO-2, SO-3) during scan testing, using control inputs (CTL-1, CTL-2, CTL-3) and enable inputs (Enable-1, 2, 3) associated with wrappers 307-309, Figure 6b. Also, see Col. 5, lines 35-45, for describing instruction scan operations.

An input side sub logic circuit unit (input linking circuitry 602) receives a serial input (SI 604) for dynamic simulation testing coupled to the input ports (SI-1, SI-2, SI-3) of the core block (cores 1-3) that generates sub data for the input ports. The wrapper serial outputs (SO-1, SO-2, SO-3) are also input to the input linking circuitry 602.

MUX unit, such as multiplexers (608-610), that selectively provides connections between the serial inputs (SI-1, SI-2, SI-3) of wrappers 307-309 and signals SI 604,

(SO-1, SO-2, and SO-3). Multiplexers 608-610 receive linking control (SELSI-1, SELSI-2, SELSI-3) inputs from Link bus 606, Figure 6B.

Regarding Claims 2, 5, an output side sub logic circuit unit (output linking circuitry 603) coupled to the plurality of output ports serial outputs (SO-1, SO-2, SO-3) that outputs final serial output 605,

Regarding Claim 3, wherein the MUX unit comprises a plurality of multiplexers (608-610) associated with the input ports (SI-1, SI-2, SI-3), as illustrated in Figure 6B.

Regarding Claims 6-12, 17-19, 22-24, wherein the core block comprises a first core logic circuit unit (CORE 1) that generates the core internal data (SO-1) an a scan test circuit unit wrappers (307) coupled to (CORE 1) and the vector input terminal (SO-1) that is configured to output the core internal data during scan testing and to selectively output data using MUX 608. The core block further comprises a second core logic circuit unit (CORE 2) coupled to wrappers (308) that generates the core output data (SO-2). The wrapper is in compliance with the IEEE 1149.1 boundary scan architecture. For example, Figure 1 illustrates the test structure of a prior art wrapper 100, which includes test interface signals 109, an instruction register 105, and set of data registers 106-108. The instruction register is a register accessed by the test interface signals to load test instructions that control the operation of the wrapper, in particular the instructions control the selection of a data register and control the mode of operation of the selected data register.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2138

By: 2/17/2006

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